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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte WOOGEUN RHEE, DANIEL FRIEDMAN,
and MEHMET SOYUER

Appeal 2007-4281
Application 10/697,751
Technology Center 2800

Decided: April 17, 2008

Before JOSEPH F. RUGGIERO, ROBERT E. NAPPI, AND JOHN A. JEFFERY, *Administrative Patent Judges*.

NAPPI, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 6(b) from the final rejection of claims 1 through 15.

We affirm-in-part the Examiner's rejection of these claims.

INVENTION

The invention is directed to a phase interpolation technique for voltage controlled delay line implementation. The invention employs a second order phase interpolation to improve tuning range over a full 180

degrees. See page 1 of Appellants' Specification. Claim 9 is representative of the invention and reproduced below:

> 9. A method for delaying an input signal, comprising the steps of:
> obtaining an input signal and a complement of the input signal; and
> using the input signal and the complement of the input signal to perform a phase interpolation process so as to realize a complete delay tuning range with respect to the input signal.

REFERENCES

Anderson	US 6,122,336	Sep. 19, 2000
Garlepp	US 6,133,773	Oct. 17, 2000
Kim	US 6,295,328 B1	Sep 25, 2001

REJECTIONS AT ISSUE

Claims 1 through 6 and 9 through 14 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Anderson. The Examiner's rejection is on pages 3 and 4 of the Answer.

Claim 15 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Garlepp. The Examiner's rejection is on page 4 of the Answer.

Claims 7 and 8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Anderson in view of Kim. The Examiner's rejection is on pages 5 and 6 of the Answer.

Throughout the opinion, we make reference to the Brief (received June 13, 2007) and the Answer (mailed May 22, 2006) for the respective details thereof.

ISSUES

Rejection under 35 U.S.C. § 102(b) based on Anderson.

Appellants contend that the Examiner's rejection of claims 1 through 6 and 9 through 14 under 35 U.S.C. § 102(b) as being anticipated by Anderson is in error. Appellants argue that Anderson does not teach the use of an input signal and its complement. Appellants reason that the signals $A\varphi_0$ and $A\varphi_4$ are clock signals, not input signals. Appellants also argue that Anderson does not provide a "complete delay tuning range with respect to the independent input signal."

Thus, Appellants' contentions with respect to independent claims 1 and 9 are whether the Examiner erred in finding that Anderson teaches an input signal and its complement and whether Anderson's device provides a complete delay tuning range. Appellants' arguments raise additional points with respect to dependent claims 2 through 6 and 10 through 14 which we will address in our analysis.

Rejection under 35 U.S.C. § 102(b) based on Garlepp.

Appellants contend that the Examiner's rejection of claim 15 under 35 U.S.C. § 102(b) as being anticipated by Garlepp is in error. Appellants argue that Garlepp does not teach the use of an input signal and its complement. Further, Appellants also argue that Garlepp does not provide a "complete delay tuning range with respect to the independent input signal."

Thus, Appellants' contentions with respect to claim 15 are whether the Examiner erred in finding that Anderson teaches an input signal and its complement and whether Anderson's device provides a complete delay tuning range.

Rejection under 35 U.S.C. § 103(a) based on Anderson and Kim.

Appellants argue on page 9 of the Brief that the Rejection of claims 7 and 8 is in error. Appellants reason, "[b]ased at least on the remarks above with respect to Anderson in terms of claims 1 and 9, it is clear that Anderson fails to disclose these limitations [limitations directed to input signal, its complement and complete delay tuning range]." Br. 9. Further, Appellants argue that the "Office action fails to provide sufficient rationale for the motivation to combine the two references." *Id.* Appellants do not elucidate as to why the Examiner's rationale is insufficient.

Thus, the Appellants' contentions present the same issues as presented with respect to claims 1 and 9. Further Appellants' contentions present us with the issue of whether the Examiner has provided a rationale for the motivation to combine the references.

FINDINGS OF FACT

1. Anderson teaches a digital clock recovery circuit which includes a phase interpolation unit which increases the number of clock phases. The circuit also includes a phase selector. Abstract.
2. In Anderson's device a frequency synthesizer inputs N clock phases into a phase interpolator unit. The phase interpolator unit includes two series connected phase interpolators, which use the N clock phases to create 2N (out of the first stage, 312) and 4N (out of the second stage, 314) clock phases. Figure 3.
3. In Anderson's device when N is 8, the frequency synthesizer inputs onto the phase interpolator, 8 signals each separated by a 45

degree delay. The output of the first phase interpolator has 16 signals each separated by a 22.5 degree delay, and the output of the second interpolator has 32 signals each separated by 11.25 degrees. Figures 4, 5, and 6; col. 4, ll. 13-26.

4. Anderson uses the output signals of the second interpolator in comparison with the data to be sampled to determine which of the output signals is optimal to be used as the sampling clock. Col. 4, ll. 27-55.
5. Garlepp teaches a method and apparatus for an adjustable delay interpolator. Abstract.
6. In one embodiment, depicted in Figure 7, two clock signals (750,770) and their complements (760, 780) are inputted into a phase interpolator. Garlepp, col. 6, ll. 62-67.
7. Garlepp teaches that the phase interpolator allows the phase to be adjusted to any phase between the two clock signals (750 &770). Col. 7, ll. 1-4.

ANALYSIS

Rejection under 35 U.S.C. § 102(b) based on Anderson.

Appellants' arguments have not persuaded us that the Examiner's rejection of independent claims 1 and 9 under 35 U.S.C. § 102(b) is in error. Appellants address independent claims 1 and 9 together, thus we consider claim 9 to be representative of the group of claims 1 and 9. Independent claim 9 recites a "obtaining an input signal and a complement of the input signal" and using the input signals "to perform a phase interpolation process." The Examiner states, on page 7 of the Answer, that Anderson's

signals $A\varphi_0$ and $A\varphi_4$ are signals input to phase interpolators, and that there is no "requirement in the claims that the input signal and complement of the input signal be [a] non-clock signal or a particular type of signal." Ans. 7. We concur with the Examiner's claim interpretation, as we find that the only limitation in claim 9 directed to the signals is that they are input to a phase interpolator and that one is the complement of the other.

We find that Anderson teaches that signals $A\varphi_0$ and $A\varphi_4$, are both input into a phase interpolator. Fact 2. That these signals are clock signals is of no consequence as they are input to phase interpolators and as such constitute input signals. Further, signal $A\varphi_4$ is 180 degrees out of phase with signal $A\varphi_0$ (i.e. signal $A\varphi_4$ is a logic level high when signal $A\varphi_0$ is logic level low) and as such $A\varphi_4$ is the complement of $A\varphi_0$ (see Figure 4). Thus, Appellants' arguments have not persuaded us that the Examiner erred in finding that Anderson teaches an input signal and its complement as claimed.

Further, we are not persuaded of error by Appellants' arguments that Anderson's device does not provide a complete delay tuning range as claimed. Claim 9 additionally recites "to realize a complete delay tuning range with respect to the input signal." Appellants assert, on page 6 of the Brief, that the Specification defines this complete delay tuning range as a tuning range of 180 degrees. The Examiner appears to concur with this claim interpretation and finds that Anderson teaches this range through the process of delaying and interpolating. As there is no disagreement of the meaning of the term "complete delay tuning range" we accept that the scope of this term includes "a tuning range of 180 degrees."

We concur with the Examiner's finding that the phase interpolation process of Anderson teaches a tuning range of 180 degrees. Anderson uses the input signals to the interpolators, which includes a signal $A\varphi_0$ and its complement $A\varphi_4$, to produce 4 times the number of signals. Fact 2. The output of the second interpolator presents 32 signals, each delayed 11.25 degrees from the prior, and thus each output signal is delayed a multiple of 11.25 degrees from signal $A\varphi_0$. Fact 3. Thus, the signals encompass at least 180 degrees of phase delay in 11.24 degree increments. One of these output signals is selected to be the clock for sampling data. Fact 4. Thus, through the selection of one of the interpolated signals, the device is able to adjust the delay of the input signal $A\varphi_0$, in 11.25 degree increments over 180 degrees of adjustment range. Accordingly, we are not persuaded that the Examiner erred in finding that Anderson's device provides a complete delay tuning range. Accordingly, we sustain the Examiner's rejection of claims 9 and 1.

Appellants argue on page 7 of the Brief that the rejection of claims 2 and 10 is in error as it does not appear that Anderson teaches a second order phase interpolation process. In response, the Examiner states that Figure 4 of Anderson discloses that the first order is performed by phase interpolator 412 and the second order phase interpolator is performed by phase interpolator 414. Appellants have not identified in the Brief, or filed a Reply Brief which identifies, any error in the Examiner's finding that these two interpolators meet the "second order phase interpolation process" as recited in claim 10. We concur with the Examiner's finding that Anderson teaches that the phase interpolator includes two phase interpolators. Fact 3. Accordingly, we sustain the Examiner's rejection of claims 2 and 10.

Appellants argue on page 7 of the Brief that the rejection of claims 3 and 11 is in error for the reasons discussed with respect to claims 1 and 9, stating that "no where does Anderson teach or suggest a delay tuning range equivalent to 180 degrees of a period of the input signal." Ans. 7. These arguments have not persuaded us of error in the Examiner's rejection of claims 3 and 11. As discussed *supra* with respect to claim 9 we find that Anderson's device is able to adjust the delay of the input signal $A\varphi_0$, in 11.25 degree increments over 180 degrees of adjustment range. Accordingly, we sustain the Examiner's rejection of claims 3 and 11.

Appellants argue on page 7 of the Brief that the rejection of claims 4 and 12 is in error as Anderson does not appear to disclose that the delay tuning range is guaranteed over a process variation. Appellants similarly argue that the rejection of claims 5 and 13 is in error as Anderson does not appear to disclose that the delay tuning range is guaranteed over a temperature variation. In response the Examiner states:

> [I]n a broad interpretation, any device that is operable is guaranteed in some range of variations, whether temperature variation or process variation, since no system is perfect enough as to not take into consideration some level of tolerance for variations. Additionally, there is no express level or range of variations in temperature or process defined by Appellant.

Ans. 8

We concur with the Examiner's analysis. Representative claims 12 and 13 recite that the delay tuning range is guaranteed over a variation in either process or temperature. The claims do not recite any tolerances or bounds of the variation to which the method is guaranteed. As such, proper operation over any variation in either process or temperature will meet the claim, which includes the normal variances expected during operation of the

device. Further, there is no disclosure in Anderson that variations in process or temperature would impact the delay tuning range. There is no question as to whether the method or device of Anderson is operative for its intended operation (i.e. guaranteed to operate). Thus, we concur with the Examiner's finding that Anderson's method is guaranteed to meet the delay tuning range over a process or temperature variation. Accordingly, we sustain the Examiner's rejection of claims 4, 5, 12, and 13.

Appellants argue on pages 7 and 8 of the Brief that the rejection of claims 6 and 14 is in error for the reasons discussed with respect to claims 1 and 9 as "no where does Anderson teach or suggest that the complement of the input signal is used to generate an absolute 180-degree phase reference." Br. 8. These arguments have not persuaded us of error in the Examiner's rejection of claims 6 and 14. As discussed *supra* with respect to claim 9, we find that Anderson's device is able to adjust the delay of the input signal $A\varphi_0$ in 11.25 degree increments over 180 degrees of adjustment range. Accordingly, we sustain the Examiner's rejection of claims 6 and 14.

Rejection under 35 U.S.C. § 102(b) based on Garlepp.

Appellants' arguments have persuaded us that the Examiner's rejection of claim 15 under 35 U.S.C. § 102(b) is in error. Appellants argue on page 8 of the Brief that Garlepp does not teach using an input signal and its complement and that Garlepp does not teach realizing a complete delay tuning range. As discussed above with respect to claim 1, Appellants and the Examiner have agreed that the scope of the term "complete delay tuning range" is a tuning range of 180 degrees.

The Examiner, on page 9 of the Answer, refers to Garlepp's Figure 7 as showing an input signal 750 and its complement 750 coupled to a phase interpolator. We concur with this finding. Fact 6. The Examiner states that the interpolator and the delay circuit provide a complete delay tuning. We disagree with this finding by the Examiner. Garlepp teaches that the phase delay tuning is between the two input clock signals. Fact 7. For this teaching to meet the claimed complete tuning delay (a tuning range of 180 degrees) the two clock signals (750 and 770) would have to be 180 degrees apart. We find no disclosure in Garlepp of such a phase separation. Accordingly, we do not find that Garlepp teaches all of the limitations of claim 15 and we will not sustain the Examiner's rejection of claim 15.

Rejection under 35 U.S.C. § 103(a) based on Anderson and Kim.

Appellants' arguments have not persuaded us of error in the Examiner's rejection of claims 7 and 8. Appellants' arguments that the rejection of claims 7 and 8 is in error for the reasons discussed with respect to claims 1 and 9, is not persuasive for the reasons discussed *supra* with respect to claims 1 and 9. Further, Appellants' statement that the Examiner has failed "to provide sufficient rationale for the motivation to combine the references" (Br. 9) is not persuasive of error. The Examiner has stated, on page 5 of the Answer, that the combination would simplify construction and provide high operational safety. Appellants have provided no argument or evidence to show that this finding by the Examiner is in error. In the absence of such argument and evidence, we find the Examiner's finding to be sufficient and sustain the Examiner's rejection of claims 7 and 8.

ORDER

For the foregoing reasons, we will not sustain the Examiner's rejection of claim 15 under 35 U.S.C. § 102(b). However, we affirm the Examiner's rejection of claims 1 through 6 and 9 through 14 under 35 U.S.C. § 102(b) and claims 7 and 8 under 35 U.S.C. § 103(a). The decision of the Examiner is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

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